REMARKS

1. The final office action is believed to be ***premature*** because it contains a new ground of rejection: Claims 1, 4, 7-9 are rejected under 35 U.S.C. 102(b) over U.S. patent 6,787,415 to Chung et al. MPEP 706.07(a) states:

> ... a second or any subsequent action on the merits ... will not be made final if it includes a **rejection, on newly cited art**, other than information submitted in an information disclosure statement filed under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17 (p), of any claim not amended by applicant ...

The Examiner is requested to withdraw the finality of the Office Action (see MPEP 706.07(d)).

2. The rejection of Claims 1, 4, 7-9 under 35 U.S.C. 102(b) over Chung et al. is traversed for the following reasons.

Claim 1 is supported by the original disclosure as follows:

> (a) forming ... first conductive gates **(select gates 144S in Figs. 3B, 18A)** ..., the first conductive gates being spaced from each other and not electrically interconnected **(at the stage of Fig. 18A)**;
>
> ...
>
> (d) forming at least one conductive line **(WL 144, Fig. 3B)** electrically interconnecting two or more of the first conductive gates.

Claim 1 is not limited to the embodiments discussed herein.

Claim 1 thus recites in paragraph (d) that a "conductive line" electrically interconnects first conductive gates which are not electrically interconnected at the stage of paragraph (a) of Claim 1.

The Examiner reads Applicant's first conductive gates on Chung's wordlines 160 of Fig. 3B, and Applicant's first conductive line on Chung's metal strap line 320. This is inappropriate for the following reason. Chung's strap line 320 "runs over the corresponding wordline 160 and electrically contacts the wordline ... at periodic intervals" to reduce the

resistance between different wordline portions (column 3, lines 30-38). The wordline portions electrically interconnected by strap line 320 were also interconnected by wordline 160 itself (at the stage of Fig. 7; see column 5, lines 9-31) before the strap line was formed. Chung does not teach or suggest that a strap line 320 may electrically interconnect different wordlines 160 that were not electrically interconnected at some stage before the strap line was formed as recited in Claim 1. Nor does Chung provide a motivation for such a strap line.

Claims 4, 7-9 depend from Claim 1.

3. Claims 2-3 and 5-6 were rejected under 35 U.S.C. 103 over U.S. patent 5,543,339 to Roth et al.

Claims 2-3 and 5-6 depend from Claim 1. Claim 1 is believed to be allowable over Roth for the following reasons.

Claim 1 is supported by the original disclosure as follows:

> (a) forming ... first conductive gates **(select gates 144S in Figs. 3B, 18A)** ..., the first conductive gates being spaced from each other and not electrically interconnected **(at the stage of Fig. 18A)**;
>
> (b) forming ... conductive floating gates **(FG 120)** ...;
>
> (c) forming ... conductive gate lines **(control gate lines CG 134, Figs. 3A, 3B, 3F)** each of which provides second conductive gates for one column of the memory cells ...;
>
> (d) forming at least one conductive line **(WL 144, Fig. 3B)** electrically interconnecting two or more of the first conductive gates.

In the embodiment of Figs. 3A-3F and 18A, wordlines 144 are formed from a different layer than the select gates 144S interconnected by the wordlines 144. Therefore, additional control is provided over the vertical spacing between the wordlines 144 and the control gate lines 134 (specification, page 2, paragraph [0009]), and hence the parasitic capacitance between the wordlines and the control gate lines can be reduced. Of course, it is well known that the capacitance between two features can be reduced by increasing the spacing between the features. However, increasing the (horizontal) spacing between the

select gates and the control gates can lead to an undesirable increase of the memory size. Applicant has realized that the spacing can be increased vertically if the wordlines are made from a different layer. Using a different layer for a conductive line interconnecting different features is generally considered undesirable because of alignment tolerances needed for the contact openings to connect the conductive line to the different features (e.g. to select gates 144S), but some embodiments of the invention provide self-aligned contacts.

Claim 1 is not limited to the embodiments described herein.

Claim 1 was rejected under 35 U.S.C. 102 over Roth in the previous Office Action, issued June 29, 2005. In reply, Applicant explained in the Amendment dated September 22, 2005, on pages 7-8, how Claim 1 distinguished over Roth. In particular, Roth's word lines and control gates are formed from the same layer 91, and Roth does not disclose a processing stage in which the individual control gates are not electrically interconnected as recited in paragraph (a) of Claim 1. Moreover, Roth is not directed to the problem of reducing the parasitic capacitance between the word line 91 and other gates. Roth discloses in column 5, lines 61-62 that the word line 91 could be modified to provide "merged select/control gates", and this disclosure teaches away from reducing the capacitance between the select and control gates as in some embodiments of Claim 1. Roth also mentions in column 6, lines 1-2 that "separate select and control gates may be used, but typically results in a large cell size." Roth thus discourages the use of separate select and control gates and does not address the capacitance problem, providing no motivation for Applicant's invention.

With respect to Claims 2-3 and 5-6, the Examiner states that "the selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results", citing *In re Burhans*, 69 USPQ 330 (CCPA 1946). The *In re Burhans* decision addressed steps of preparing wheat flour for baking (separating the wheat germ, impregnating the flour with silicon dioxide, etc.) The order of steps in preparing flour for baking involves different considerations than in fabrication of semiconductor integrated circuits. For example, Claim 2 recites that "the first conductive gates are formed before the floating gates". In Roth (Fig. 8), the word line 91 (providing the control gates) is formed on

the sidewalls of oddly shaped floating gates. Each floating gate is formed of members 13, 22, 31 (column 3, last three lines, and column 4, line 1). Each floating gate has a cavity, and the wordline is present both inside and outside the cavity. Roth does not teach, suggest, or enable one skilled in the art to form this structure with a reverse order of fabrication steps (i.e. by forming the word line 91 before the floating gates) as recited in Claim 2. Hence, Roth does not make the reverse step order prima facie obvious.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 6, 2006.

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